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09/662,068	09/14/2000	Gerry R. Talbot	0939A-036911US	1454

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EXAMINER	
DINH, NGOC V	

ART UNIT	PAPER NUMBER
2187	11

DATE MAILED: 10/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PRG

Office Action Summary	Application No.	Applicant(s)	
	09/662,068	TALBOT ET AL.	
	Examiner	Art Unit	
	NGOC V DINH	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *53,54 and 56-70* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *53-54, 56-70* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This Office Action is responsive to Amendment filed 7/28/03 in which claim 55 is canceled, claims 69-70 are added.

Applicant's previous arguments are moot with regard to claims 53-54, 56-68 in view of the new rejection. Claims 53-54, 56-70 are also subject to obviousness-type double patenting as being unpatentable over claims 1-15 of U.S. Patent No. 6,272,600 Talbot et al.

ACKNOWLEDGEMENT OF REFERENCE CITED BY APPLICANT

2. As required by M.P.E.P. 2001.06(b) and C.F.R 1.98(d) since the instant application has been identified as a continuation application of: an earlier filed application No. 60031063, now patent No. 6272600, and application No. 08808849, now patent No. 6272600, and is relied upon for an earlier filing date under 35 U.S.C. 120, the Examiner has reviewed the prior art cited in the earlier related application as required by M.P.E.P 904.

CLAMS REJECTION - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 53 is rejected under 35 U.S.C.102 (e) as being anticipated by Wang et al. [5,642,494].

3. As per claims 53:

Wang teaches in a data processing system, a method for ordering a plurality of memory access requests, the method comprising: accepting the plurality of memory access requests (write requests in column 3 line 8 and read requests in column 3 line 12);

determining the availability or memory locations for first and second memory requests from the plurality of requests, prior to scheduling or reordering either the first or the second memory request (i.e., while one request being serviced already, the subsequent request is serviced next in order to compare its conflicts with the previous one; see column 3 lines 1-7, also, Wang's cache memory is designed to accept a plurality of memory access requests as well; see write requests in column 3 line 8 and read requests in column 3 line 12), and ordering for determining execution order module [backside queue FIFO (240), fig. 2] from receiving order [col. 5, lines 35-50]; a result ordering module for returning results of execution unit according to receiving order [e.g., FIFO queue], and an execution unit for executing plurality of memory access requests in execution order ordering the plurality of memory access requests [col. 3, lines 1-2] wherein a first request of the plurality of memory access requests to an available memory location or availability of target memory addresses (i.e., the request not being blocked) precedes a second request of the plurality of memory access requests to an unavailable memory location (i.e., the memory request being blocked; giving the priorities to the access requests which hits the cache memory while blocking the access requests for a nonavailable memory location; see column 3 lines 2-7), and after the ordering, servicing the first request [col. 3, lines 1-15; col. 7, lines 22-35; col. 16, lines 1-25].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 56, 59-64, 66 are rejected under 35 U.S.C 103(a) as being unpatentable over Wang, and in view of a well known feature of which official notice is hereby taken.

4. As per claim 56, 60-61:

Wang teaches in a data processing system, a method for processing a plurality of memory access request, the method comprising: receiving the plurality of memory access

requests by a queue (see column 3 lines 1-2); **ordering** plurality of memory access requests in the queue based on the availability of target memory addresses (i.e., the request not being blocked) associated with a memory access request of the plurality of memory access requests; a first memory access request with an available target memory address preceding a second memory access request with an unavailable target memory address [col. 3, lines 1-15]; and after the ordering, servicing plurality of access requests, after servicing of plurality of memory access requests, returning results of servicing according to a received order of plurality of memory access requests by queue (e.g., order module [backside queue FIFO (240), fig. 2) [col. 3, lines 1-15; col. 7, lines 22-35; col. 16, lines 1-25].

Wang does no teach **reordering** plurality of memory access requests in the queue. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include the reordering method into Wang's processing system. Doing so would allow the requests in the queue being reordered from time to time so the request with high priority being processed first, therefore the access latency is reduced. Furthermore, reordering is a well-known method in the art, wherein the requests stored in the queue are reordered from time to time so as the requests with high priority will be served first.

5. As per claim 59, 64:

Wang teaches the claimed limitation as noticed above.

Wang does not teach queue is a priority queue. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include priority queue into Wang computer system so as requests with different priority level will be stored in different queues priority level, therefore reducing memory access latency. In general, a software systems often utilize a priority queue of entities sorted by some set of comparison criteria. The entities may represent tasks that a software system must perform or data that a software system must process. The priority queue is utilized to order those tasks. The entity at the top of the priority queue is the most critical entity. This entity represents the task that the software system should perform next. A software system utilizing the priority queue removes the most critical entity from the priority

queue and executes tasks appropriate to that entity. The software system then resorts the priority queue listing the remaining entities in order of importance. The most critical entity again occupies the top spot of the priority queue.

6. As per claim 66:

Wang does not teach plurality of memory access requests comprises at least three memory access requests. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made because the number of memory access requests with available target memory addresses can be any number depend on how heavily the system memory is in used at the time the requests are issued.

7. As per claim 67:

Wang teaches a results ordering module [e.g., FIFO queue; (240), fig. 2] for returning results of execution unit according to receiving order.

8. As per claims 68-70:

Wang teaches the claimed limitation as noticed above.

Wang does not teach ordering plurality of memory access requests, wherein a first request to a first **memory bank** that is not currently being accessed (**available memory bank**) precedes a second request to a second **memory bank** that is currently being accessed (**unavailable memory bank**); reordering plurality of memory access requests based on the availability of target memory addresses, wherein a target memory address is available if it is located in a **memory bank** that is not currently being accessed (e.g., available memory bank). However, it would have been obvious to one having ordinary skill in the art at the time the invention was made because multi-bank memory is a well-known architectures in semiconductor memory device, wherein the semiconductor memory device comprising a plurality of memory bank groups. Each memory bank group comprises a plurality of memory banks arranged in a stacked-bank architecture allows greater memory capacity by accommodating multiple memory banks.

9. As per claims 62-63:

Wang teaches the method of steps in claims 53-54, 56-61, therefore Wang teaches the data processing system in claims 62-63.

Claims 54, 57-58, 65 are rejected under 35 U.S.C 103(a) as being unpatentable over Wang.

10. As per claims 54, 57-58, 65:

Wang teaches the claimed limitation as mentioned above.

Wang does not teach plurality of memory access requests comprises at least three memory access requests; reordering provides for at least two memory access requests with available target memory addresses, and the servicing is done sequentially. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made because the number of memory access requests with available target memory addresses can be any number depend on how heavily the system memory is in used at the time the requests are issued. The reordering process will reorder the requests in the queue from highest to lowest priority level, then the servicing request will be done sequentially from highest priority request to lowest priority request.

DOUBLE PATENTING

Claims 53-54, 56-70 rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-15 of U.S. Patent No. 6,272,600 Talbot et al.

11. As per claims 53, 56, 61-63, 68-69:

Talbot [6272600] teaches in a data processing system, a method for **reordering** a plurality of memory access requests, the method comprising: accepting the plurality of memory access requests; **reordering** the plurality of memory access requests, wherein a first request [e.g., at least one memory access request] of the plurality of memory access requests to an available memory location or availability of target memory addresses precedes a second request [e.g., at least one memory access request] of the plurality of memory access requests to an unavailable memory location; execution unit for executing access requests [e.g., non-available]; [Talbot (6272600), claims 1-20];

after servicing of plurality of memory access requests, returning results of servicing according to a received order of plurality of memory access requests by queue [Talbot (6272600), col. 12, lines 45-46];

An availability determiner for determining availability of memory locations requested by plurality of memory access requests [Talbot (6272600), claim 8-9].

Talbot [6272600] does not specifically teach **ordering** a plurality of memory access requests. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made because the reordering process already include the ordering step. When requests are first received, they are received in an initial order in the queue, then the queue logic order would reorder the requests from time to time so the high priority requests would be serviced first.

Implicitly, Talbot [6272600] teaches after the **reordering**, servicing the first request through the scheduling [claims 1, 3-4]. This is because the purpose of reordering step is first to select requests which have higher priority [e.g., particular operation] then service those requests with higher priority before service request with lower priority [Talbot, claim 3].

As mentioned above Talbot teaches the reordering method based on the **available** [not currently being accessed]/**unavailable** [currently being accessed] **memory locations**, and determining whether the memory bank is available [Talbot, col. 13, lines 40-43]. Talbot [6272600] does not specifically teach **ordering** a plurality of memory access requests wherein a first request [e.g., at least one memory access request] of the plurality of memory access requests to a **first memory bank** that is not currently being accessed precedes a second request of the plurality of memory access requests to a **second memory bank** that is currently being accessed. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made because the memory locations also contain the memory banks, therefore reordering requests into available/unavailable memory locations means reordering requests into available/unavailable memory banks.

12. As per claims 54, 57-60, 65, 67, 70:

Talbot [6272600] implicitly teaches: access requests comprises at least three memory access requests; reordering provides for at least two memory access with available target memory addresses [e.g., plurality of memory access requests]; servicing is done sequentially. This is because the number of memory access request is no more than a

matter of the capacity of the request queue and the reordering method would move the request with high priority to the top of the queue, and the requests would be served sequentially from highest to lowest priority request; queue is a priority queue, this is a well known feature in the art that queues are categorized into low/high priority level just like memory access requests, wherein high priority requests reside in high priority queue, and low priority requests reside in low priority queue.

13. As per claims 64, 66:

Talbot teaches a **reordering** module for determining execution order from receiving order; an execution unit for executing plurality of memory access requests in execution order [claims 1-3].

Talbot does not teach an **ordering** module for determining execution order from receiving order. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made because the reordering process already include the ordering step. When requests are first received, they are received in an initial order in the queue, then the queue logic order would reorder the requests from time to time so the high priority requests would be serviced first.

Conclusion

14. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Ngoc Dinh whose telephone number is (703) 305- 3032. The examiner can normally be reached on Monday-Friday 8:30 AM-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A. Sparks, can be reached on (703) 308-1756. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

NGOC DINH
Patent Examiner
ART UNIT 2187
September 23, 2003

DONALD A. SPARKS
Supervisor Patent Examiner
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